Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A method of digital communication between two devices, said method comprising the steps of:

(1) a control device transmitting a clock signal, a frame signal and an instruction to transmit a predetermined bit pattern;

(2) a target device, responsive to receipt of said instruction to transmit a predetermined bit pattern and responsive to receipt of said frame signal, transmitting said predetermined bit pattern using said received clock signal;

~~(1) a first device transmitting a predetermined bit pattern to a second device responsive to an instruction to transmit said predetermined bit pattern in a first time slot of a next frame and a start of said next frame signal transmitted from said second device using a clock signal transmitted from said second device;~~

~~(2) said second device sampling for bits of said predetermined bit pattern at sampling times determined by one of a rising edge or a falling edge of said clock signal as a function of beginning a delay period after said start of said next frame signal;~~

(3) said control device sampling for bits of said predetermined bit pattern at predetermined sampling times;

([[3]] 4) if said ~~second~~ control device does not detect said predetermined bit pattern, ~~increasing said~~ adding a delay ~~period by~~ of a fraction of a clock period to said predetermined sampling times and repeating steps (1) ~~and~~ (2) and ~~if necessary, step~~ (3);

([[4]] 5) if said ~~second~~ control device detects said predetermined bit pattern, setting ~~the last~~ a sum of all said delays added in step 4 ~~delay period used in step (2)~~ as a delay period to be used by said ~~second~~ control device for sampling data for further transmissions from said ~~first~~ target device to said ~~second~~ control device;

([[5]] 6) said ~~second~~ control device using said ~~last~~ delay period for sampling all further data transmissions from said first device to said second device; and,

wherein said ~~second~~ control device performs step ([[2]] 3) twice before proceeding to steps ~~(3) or~~ (4) or (5).

2. (cancelled)

3. (currently amended) The method of claim 1 wherein said ~~start of said next~~ frame signal is a frame synchronization signal denoting a beginning of a frame.

4. (cancelled)

5. (currently amended) The method of claim 1 wherein said ~~start of said next~~ frame signal is transmitted on a first signal line, said predetermined bit pattern and all further data is transmitted on a second signal line and a clock signal is transmitted on a third signal line and wherein transmissions on said second signal line and said predetermined sampling times are also a function of said clock signal.

6. (cancelled).

7. (currently amended) The method of claim [[6]] 5 wherein said clock signal is generated at said ~~second~~ control device.

8. (cancelled).

9. (cancelled).

10. (currently amended) The method of claim 5 wherein, in step ([[3]] 4), said delay is ~~increased by~~ one-half of a clock cycle.

11. (cancelled).

12. (currently amended) A method of digital communication between two devices, said method comprising the steps of:

~~(1) a first device transmitting a predetermined bit pattern to a second device responsive to an instruction to transmit said predetermined bit pattern in a first time slot of a next frame and a start of said next frame signal transmitted from said second device using a clock signal transmitted from said second device;~~

(1) <u>a control device transmitting a clock signal, a frame signal and an instruction to transmit a predetermined bit pattern;</u>

(2) <u>a target device, responsive to receipt of said instruction to transmit a predetermined bit pattern and responsive to receipt of said frame signal, transmitting said predetermined bit pattern using said received clock signal;</u>

~~(2) said second control device sampling for bits of said predetermined bit pattern at sampling times determined by one of a rising edge or a falling edge of said clock signal beginning a delay period after said start of said next frame signal;~~

<u>(3) said control device sampling for bits of said predetermined bit pattern at predetermined sampling times;</u>

([[3]] 4) if said ~~second~~ <u>control</u> device does not detect said predetermined bit pattern, ~~increasing said~~ <u>adding a</u> delay ~~period by~~ <u>of</u> a fraction of a clock period <u>to said predetermined sampling times</u> and repeating steps (1) ~~and~~ (2) and ~~if necessary, step~~ (3);

([[4]] <u>5</u>) if said ~~second~~ <u>control</u> device detects said predetermined bit pattern, setting ~~the last~~ <u>a sum of all said delays added in step 4</u> ~~delay period used in step (2)~~ as a delay period to be used by said ~~second~~ <u>control</u> device for sampling data for further transmissions from said ~~first~~ <u>target</u> device to said ~~second~~ <u>control</u> device;

([[5]] <u>6</u>) said ~~second~~ <u>control</u> device using said ~~last~~ delay period for sampling all further data transmissions from said first device to said second device; and,

([[6]] <u>7</u>) said ~~first~~ <u>target</u> device predicting arrival of said ~~start~~ <u>frame</u> signal and commencing transmission of data in anticipation of receipt of ~~said start of said next~~ frame signal.

13. (currently amended) A communication device for receiving digital data from another device, said communication device comprising:

a receive port for receiving data transmitted to said communication device from ~~another~~ a target device;

a processor adapted to:

(a) sample data received at said receive port for a predetermined bit pattern at predetermined sampling times ~~determined by one of a rising edge or a falling edge of a clock signal~~ ~~beginning a delay period after a start of a next frame signal, said~~ ~~start of a next~~ and wherein a frame signal transmitted by said communication device ~~and initiating~~ initiates transmittal of said predetermined bit pattern by said ~~other~~ target device using a clock signal transmitted from said ~~second~~ communication device;

~~(b) if said communication device detects said predetermined bit pattern, setting the delay period last used in step (a) as a delay period to be used by said communication device for sampling data; and~~

([[c]] b) if said communication device does not detect said predetermined bit pattern, ~~increasing said~~ adding a delay ~~period by~~ of a fraction of a clock period to said predetermined sampling times and repeating step (a) ~~and step (b) or (c)~~;

(c) if said communication device detects said predetermined bit pattern, setting a sum of all said delays added in step (b) as a delay period to be used by said communication device for sampling data; and

(d) using said ~~last~~ delay period for sampling further data transmissions; and

wherein said processor performs step (a) twice before proceeding to steps (b) or (c).

14. (currently amended) The communication device of claim 13 further comprising:

means for generating said ~~start of a next~~ frame signal; and

a second port for transmitting said ~~start of a next~~ frame signal to ~~another~~ said target device.

15. (currently amended) The communication device of claim 13 wherein said ~~start of a next~~ frame signal is a frame synchronization signal denoting a beginning of a frame.

16. (currently amended) The communication device of claim 14 further comprising means for generating said clock signal; and

a third port for transmitting said clock signal to said ~~other~~ target device and wherein transmission of said predetermined bit pattern and said sampling times also are a function of said clock signal.

17. (previously presented) The communication device of claim 16 wherein said digital communication is carried out under the control of a controller and is conducted between at least one target device.

18. (cancelled).

19. (original) The communication device of claim 13 wherein said processor is further adapted to transmit an instruction to said other device, responsive to which said other device transmits said predetermined bit pattern.

20. (currently amended) A method of receiving digital communication at a receiving device, said method comprising the steps of:

(1) receiving from a transmit device a predetermined bit pattern sent in response to a ~~start of a next frame~~ signal transmitted from said receiving device using a clock signal transmitted from said receiving device;

(2) sampling for bits of said predetermined bit pattern at predetermined sampling times ~~determined by one of a rising edge or a falling edge of said clock signal beginning delay period after said start of a next frame signal~~;

(3) if said predetermined bit pattern is not detected, ~~increasing said delay period by~~ adding a delay of a fraction of a clock period to said predetermined sampling times and repeating steps (1) and (2)~~, and, if necessary, step (3~~);

(4) if said predetermined bit pattern is detected, setting a sum of all said delays added in step (3) ~~last said delay period used in step (2)~~ as a delay period to be used for sampling data for further transmissions from said transmit device;

(5) using said ~~last~~ delay period for sampling further data communications from said transmit device; and,

wherein said second device performs step (2) twice before proceeding to steps (3) or (4).

21. (currently amended) A method of receiving digital communication at a receiving device, said method comprising the steps of:

(1) receiving from a transmit device a predetermined bit pattern sent in response to a ~~start of a next frame~~ signal transmitted from said receiving device using a clock signal transmitted from said receiving device;

(2) sampling for bits of said predetermined bit pattern at predetermined sampling times ~~determined by one of a rising edge or a falling edge of said clock signal beginning delay period after said start of a next frame signal~~;

(3) if said predetermined bit pattern is not detected~~, increasing said delay period by~~ adding a delay of a fraction of a clock period to said predetermined sampling times and repeating steps (1) and (2)~~, and, if necessary, step (3~~);

(4) if said predetermined bit pattern is detected, setting a sum of all said delays added in step (3) ~~last said delay period used in step (2)~~ as a delay period to be used for sampling data for further transmissions from said transmit device;

(5) using said ~~last~~ delay period for sampling further data communications from said transmit device; and,

(6) said transmit device predicting arrival of said ~~start of a next~~ frame signal and commencing transmission of data in anticipation of receipt of said ~~start of a next~~ frame signal.

22. (cancelled)

23. (currently amended) The method of claim 12 wherein said ~~start of said next~~ frame signal is a frame synchronization signal denoting a beginning of a frame.

24. (canceled).

25. (currently amended) The method of claim 12 wherein said ~~start of said next~~ frame signal is transmitted on a first signal line, said predetermined bit pattern and all further data is transmitted on a second signal line and a clock signal is transmitted on a third signal line and wherein transmissions on said second signal line and said sampling times are also a function of said clock signal.

26. (previously presented) The method of claim 25 wherein said digital communication is carried out under the control of a controller and is conducted between at least one target device.

27. (currently amended) The method of claim 26 wherein said start of said ~~next~~ frame signal and said clock signal are generated at said second device.

28. (cancelled).

29. (currently amended) The method of claim 12 wherein step (1) is performed responsive to receipt of an instruction from said ~~second~~ <u>control</u> device.

30. (currently amended) The method of claim 25 wherein, in step (3), said <u>added</u> delay is ~~increased by~~ one-half of a clock cycle.

31. (currently amended) A communication system comprising a transmitting device and a communication device,

wherein said communication device comprises:

a receive port for receiving data transmitted to
said communication device from said transmitting device;
a receiver processor adapted to:
(a) sample data received at said receive port for a predetermined bit pattern at <u>predetermined</u> sampling times ~~determined by one of a rising edge or falling edge of a clock signal beginning a delay period after a start of a next frame~~

~~signal, said start of a next~~ and wherein a frame signal transmitted by said communication device ~~and initiating~~ initiates transmittal of said predetermined bit pattern by said ~~other~~ transmitting device using said clock signal transmitted by said communication device;

~~(b) if said communication device detects said predetermined bit pattern, setting the delay period last used in step (a) as a delay period to be used by said communication device for sampling data; and~~

([[c]] b) if said communication device does not detect said predetermined bit pattern, ~~increasing said~~ adding a delay ~~period by~~ of a fraction of a clock period and repeating step (a) ~~and step (b) or (c); and~~

(c) if said communication device detects said predetermined bit pattern, adding a sum of said delays added in step (b) as a delay period to be used by said communication device for sampling data; and

(d) using said ~~last~~ delay period for sampling further data transmissions; and, wherein said transmitting device comprises a transmitter processor adapted to predicting arrival of said ~~start signal~~ frame signal and commencing transmission of data in anticipation of receipt of said ~~start of a next~~ frame signal.

32. (currently amended) The communication device of claim 31 further comprising:

means for generating said ~~start of a next~~ frame signal; and

a second port for transmitting said ~~start of a next~~ frame signal to said transmitting device.

33. (cancelled).

34. (currently amended) The communication device of claim 32 further comprising means for generating said clock signal; and

a third port for transmitting said clock signal to said transmitting device and wherein transmission of said predetermined bit pattern and said predetermined sampling times also are a function of said clock signal.

35. (previously presented) The communication device of claim 34 wherein said digital communication is carried out under the control of a controller and is conducted between at least one target device.

36. (previously presented) The communication device of claim 35 wherein said communication device is said controller and said other device is said target device.

37. (previously presented) The communication device of claim 31 wherein said receiver processor is further adapted to transmit an instruction to said other device, responsive to which said other device transmits said predetermined bit pattern.